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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/815,772	03/22/2001	Johni Chan	69907	5285

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EXAMINER	
MASON, DONNA K	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 12/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/815,772	CHAN, JOHNI	
	Examiner	Art Unit	
	Donna K. Mason	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 5-18* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 6 is objected to because of the following informalities:

In line 14, change "implement" to --implements--. Appropriate correction is required. See 37 CFR 1.75.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 14-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 14 recites the limitation "[t]he apparatus" in line 1. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 15 recites the limitation "[t]he apparatus" in line 1. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 16 recites the limitation "[t]he apparatus" in line 1. There is insufficient antecedent basis for this limitation in the claim.

7. Claims 17 and 18 inherit the deficiencies of claim 16, but should also be reviewed with regard to any antecedent basis problems that may be caused by amendments made to overcome this rejection.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 6-18 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,968,977 to Chinnaswamy, et al. ("Chinnaswamy").

With regard to claims 6 and 13, Chinnaswamy discloses an apparatus including a first hybrid switching module (Fig. 2, item 32). The first hybrid switching module includes a first hybrid switching module processor data channel (Fig. 2, item 36 (CPU1)), a first hybrid switching module main data channel (Fig. 2, item 38 (I/O1)), an input/output link data channel (Fig. 2, item 36 and 38 (EXP. PORT1 IN and EXP PORT1 OUT)), a first switch (Fig. 2, item 32) coupled to the first hybrid switching module processor data channel, and a first bridge (Fig. 3, item 6) coupled to the first hybrid switching module main data channel. As disclosed, the first switch selectively couples to the first bridge and selectively couples to the input/output link data channel, where the first hybrid switching module processor data channel is thereby selectively coupled to the first bridge allowing access over a first main bus to a first peripheral device that implements a first function, and selectively coupled to the input/output link data channel allowing access over a second main bus to a second peripheral device that implements a second function that is not redundant to the first function (*see generally*, Fig. 2, and column 8, lines 27-68 to column 10, lines 1-6). Chinnaswamy also discloses the first

hybrid switching module having further including a failure mode that couples the input/output link data channel with the first hybrid switching module bus data channel during failure allowing access to the first peripheral device providing the first function during the failure (column 4, lines 65-68 to column 5, lines 1-11), as recited in claim 13.

With regard to claims 7-12 and 14-18, *see generally* Figs. 2 and 3; and column 8, lines 27-68 to column 10, lines 1-6.

Therefore, Chinnaswamy reads on the invention as specified in claims 6-18.

10. Claims 6-18 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,014,005 to Fox, et al. ("Fox").

With regard to claims 6 and 13, Fox discloses an apparatus including a first hybrid switching module (Fig. 1, item Cross-Bar Switch 1; Fig. 5 and Fig. 5A). The first hybrid switching module includes a first hybrid switching module processor data channel (*see e.g.*, Fig. 1, Channel C of Processor 1), a first hybrid switching module main data channel (*see, e.g.*, Fig. 1, item 2 connecting Cross-Bar Switch 1 and I/O CU-3), an input/output link data channel (*see* channel connecting Crossbar Switch 1 and Crossbar Switch M), a first switch (Fig. 5 and Fig. 5A) coupled to the first hybrid switching module processor data channel, and a first bridge (Fig. 5 and Fig. 5A, decoder section) coupled to the first hybrid switching module main data channel. As disclosed, the first switch selectively couples to the first bridge and selectively couples to the input/output link data channel, where the first hybrid switching module processor data channel is thereby selectively coupled to the first bridge allowing access over a first main bus to a first

peripheral device that implements a first function, and selectively coupled to the input/output link data channel allowing access over a second main bus to a second peripheral device that implements a second function that is not redundant to the first function (Fig. 1, I/O CU-K). Fox also discloses the first hybrid switching module having further including a failure mode that couples the input/output link data channel with the first hybrid switching module bus data channel during failure allowing access to the first peripheral device providing the first function during the failure (column 1, lines 55-58 and column 3, lines 7-13), as recited in claim 13.

With regard to claims 7-12 and 14-18, *see generally* Figs. 1, 5, 5A, and 5B, and the accompanying text.

Therefore, Fox reads on the invention as specified in claims 6-18.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1, 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,014,005 to Chinnaswamy, et al. ("Chinnaswamy") in view of U.S. Patent No. 6,038,630 to Foster, et al. ("Foster").

With regard to claims 1, 3 and 5, Chinnaswamy discloses a system (Fig. 1, item 10) including: a first processor (Fig. 1, item 12) including a first processor data channel;

a first hybrid switching module (Fig. 1, item 20 and Fig. 2, item 32) including a first hybrid switching module processor data channel, a first hybrid switching module main data channel, and a first input/output link data channel, a first switch, and a first bridge, the first hybrid switching module processor data channel being coupled to the first processor data channel (*see generally*, Fig. 3). Chinnaswamy also discloses a first main bus coupled to the first hybrid switching module main data channel allowing the first processor to access a first peripheral device coupled with the first main bus to implement a first function (Fig. 2, item 38 (I/O1)); a second processor (Fig. 1, item 12) including a second processor data channel; a second hybrid switching module (Fig. 1, item 20 and Fig. 2, item 34) including a second hybrid switching module processor data channel, a second hybrid switching module main data channel, a second input/output link data channel, a second switch, and a second bridge, the second hybrid switching module processor data channel being coupled to the second processor data channel, and the second input/output link data channel being coupled to the first input/output link data channel (*see generally*, Figs. 2 and 3). Chinnaswamy also discloses a second main bus coupled to the second hybrid switching module main data channel allowing the second processor to access a second peripheral device coupled with the second main bus to implement a second function that is not redundant to the first function (Fig. 2, item 38A (I/O2)). As disclosed in Chinnaswamy, the first hybrid switching module includes a failure mode allowing the second processor to access the first peripheral device on the first main bus to implement the first function, and the second hybrid switching module includes a failure mode allowing the first processor to access the

second peripheral device on the second main bus to implement the second non-redundant function (column 4, lines 65-68 to column 5, lines 1-11).

Chinnaswamy does not expressly disclose where the hybrid switching module includes an arbiter. Foster discloses a crossbar switch having an arbiter (Fig. 3, item 235). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Foster with Chinnaswamy. The suggestion or motivation for doing so would have been to provide an enhanced shared access control approach for an integrated system (column 2, lines 4-10).

Therefore, it would have been obvious to combine Foster with Chinnaswamy to obtain the invention as specified in claims 1, 3 and 5.

13. Claims 1, 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,014,005 to Fox, et al. ("Fox") in view of U.S. Patent No. 6,038,630 to Foster, et al. ("Foster").

With regard to claims 1, 3, and 5, Fox discloses a system (Fig. 1) including: a first processor (Fig. 1, Processor 1) including a first processor data channel; a first hybrid switching module (Fig. 1, Cross-Bar Switch 1; Fig. 5, and Fig. 5A) including a first hybrid switching module processor data channel, a first hybrid switching module main data channel, and a first input/output link data channel, a first switch, and a first bridge, the first hybrid switching module processor data channel being coupled to the first processor data channel. Fox also discloses a first main bus coupled to the first hybrid switching module main data channel allowing the first processor to access a first

peripheral device coupled with the first main bus to implement a first function (Fig. 1, I/O CU-3); a second processor (Fig. 1, Processor 2) including a second processor data channel; a second hybrid switching module (Fig. 1, Cross-Bar Switch M; Fig. 5, and Fig. 5B) including a second hybrid switching module processor data channel, a second hybrid switching module main data channel, a second input/output link data channel, a second switch, and a second bridge, the second hybrid switching module processor data channel being coupled to the second processor data channel, and the second input/output link data channel being coupled to the first input/output link data channel. Fox also discloses a second main bus coupled to the second hybrid switching module main data channel allowing the second processor to access a second peripheral device coupled with the second main bus to implement a second function that is not redundant to the first function (Fig. 1, I/O CU-K). As disclosed in Fox, the first hybrid switching module includes a failure mode allowing the second processor to access the first peripheral device on the first main bus to implement the first function, and the second hybrid switching module includes a failure mode allowing the first processor to access the second peripheral device on the second main bus to implement the second non-redundant function (column 1, lines 55-58 and column 3, lines 7-13).

Fox does not expressly disclose where the hybrid switching module includes an arbiter. Foster discloses a crossbar switch having an arbiter (Fig. 3, item 235). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Foster with Fox. The suggestion or motivation for doing so would have

been to provide an enhanced shared access control approach for an integrated system (column 2, lines 4-10).

Therefore, it would have been obvious to combine Foster with Fox to obtain the invention as specified in claims 1, 3 and 5.

Response to Arguments

14. Applicant's arguments, see pages 8-10, filed October 14, 2004, with respect to the rejection of claims 1, 3, and 5 under 35 USC 103(a) in view of Sicola and Foster, and the rejection of claims 6-18 under 35 USC 102(e) in view of Sicola have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, new grounds of rejection are made in view of Chinnaswamy, Fox, and Foster.

The Examiner is persuaded that Sicola teaches away from providing access to non-redundant peripheral devices, in that Sicola specifically provides for a completely redundant configuration. However, both Chinnaswamy and Fox teach access to non-redundant peripheral devices.

Therefore, the Examiner cannot allow the claims.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent No. 4,438,494 to Budde, et al. ("Budde") discloses the features of claims 1, 3 and 5-18, but does not expressly disclose the hybrid

switching module including an arbiter, as claimed. However, Foster teaches a hybrid switching module including an arbiter as claimed.

16. A shortened statutory period for reply is set to expire THREE MONTHS from the mailing date of this communication. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this communication.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (571) 272-3629. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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